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Shift register(SISO)

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module shift\_register\_3bit (

input wire clk, // clock input

input wire rst, // synchronous reset

input wire serial\_in, // serial data input

output reg [2:0] q // 3-bit register output

);

always @(posedge clk) begin

if (rst)

q <= 3'b000; // reset all bits

else

q <= {q[1:0], serial\_in}; // shift left

end

endmodule